

CAPACITIVE VOLTAGE TRANSFORMER MODELS FOR OPTIMAL DISTANCE RELAYING PROTECTION SCHEME

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Abstract

Transients in capacitive voltage transformers (CVTs) usually employed as instrument transformer for high voltage, long distance transmission line protections have been causing a lot of damage. This is due to false or non-triggering of protective relays. A lot of techniques have been identified for reduction of the transients such as use of high value capacitors application of ferroresonance suppressed circuits resulting to the linear models of CVT (Active and Passive ferroresonance suppressed circuits AFSC and PFSC). This work employs AFSC and PFSC models and investigates how the system impedance ratio (SIR) employed CVT transient detection logic can be further used to reduce the CVT transients for optimal long distance relaying protection scheme. The result shows an improved CVT transient detection using the SIR and transient detection logic which is more precise than the past detection methods and does not penalize distance protection speed for close-in-faults.

Keywords: Capacitive Voltage Transformer, System Impedance Ratio, Active and Passive Ferroresonant Circuits, Detection logic.

1. Introduction

Very poor CVT transients have been causing serious concern for high-speed line protection schemes. When there is depressed phase voltage on the line resulting from faults, the CVT output voltage do not usually follow closely its input voltage due to the internal CVT energy storage elements such as capacitors and the inductors [1]. Since the elements take time to change their stored energy, they introduce the transient to the CVT output following a significant input voltage change. The direction of the CVT transient is usually defined as that period during, which the CVT output voltages does not match the ratio input voltage [2].

CVT transients reduce the fundamental component of the fault voltage. This decrease in the fundamental voltage component results in a decrease in the calculated line impedance. If the fundamental voltage reduction is great enough, zone 1 distance elements will undesirably pick up for out-of-section faults.

When the protective relay operates due to decrease in distance calculation resulting from a fault within that portion of line protected by a zone one element, the CVT transient is said to be tolerable. However, if the fault is located outside of that portion protected by zone 1 element and the CVT transient causes the zone 1 element to pick-up, then this CVT transient is not tolerable [3].

Two methods adopted for handling CVT transient overreach problem for output of section faults are:

- (i) To reduce the zone 1 element reach. But the problem here is that the CVT transient response for some applications require such a reduction in the zone 1 distance element reach and this will affect effective protection of zone 1.
- (ii) The second approach is to delay all zone 1 distance element operations in order to prevent the

distance element to produce a trip during the CVT transient. But this approach is undesirable since the close in fault clearance time are penalized unnecessarily [4].

This paper considers the reduction of CVT transient response by adjustment of CVT components such as the coupling capacitor and use of ferroresonance suppression circuits. Finally, it detailed the study of distance relaying during CVT transient using appropriate CVT, AFSC, and PFSC models adopting a system impedance ratio (SIR) and improved CVT transient detection logic.

2. Over view of CVT Components and Circuits for reduced CVT Transients

2.1 CVT Circuit

Fig. 1 below shows a CVT circuit, it contains the following components:

- Coupling Capacitors (C_1 and C_2)
- Compensation reactor (L)
- Step down transformer
- Ferroresonance - suppression circuit.

If the CVT is equipped with communication carrier, there will be addition drain coil, choke coil, and carrier switch which are as shown if fig. 1.

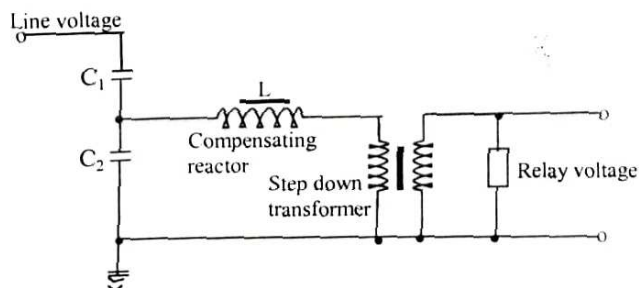


Fig. 1: CVT structure

If a fault suddenly reduces the line voltage, the CVT secondary output does not instantly follow the primary voltage. This is due to the fact that the energy stored element, such as coupling capacitors, compensating reactors cannot charge their charges or flux instantaneously and hence the resultant CVT transient.

Fig. 2 and fig. 3 below show two CVT transients for zero crossing and peak point-on-wave (POW) fault initiation. The transient of fig. 2 lasted for 1.75 cycles and fig. 3 for 1.25 cycles after fault initiation.

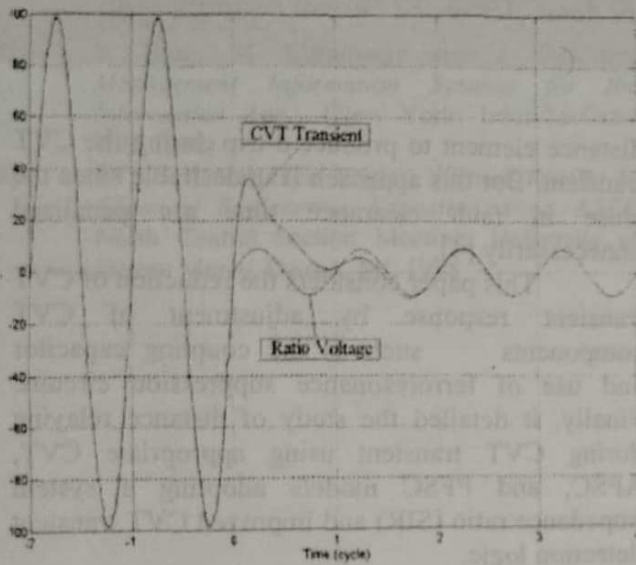


Fig. 2: CVT transient with fault at voltage zero

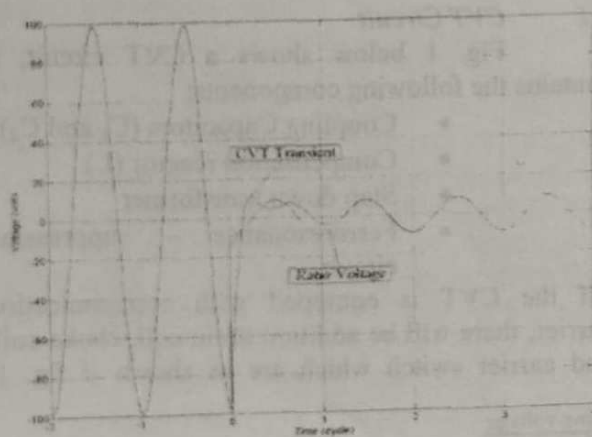


Fig. 3: CVT transient with fault at voltage peak

Fig. 4 shows the effect of high capacitive CVT. There is very high reduction of the CVT transient when compared to fig. 2.

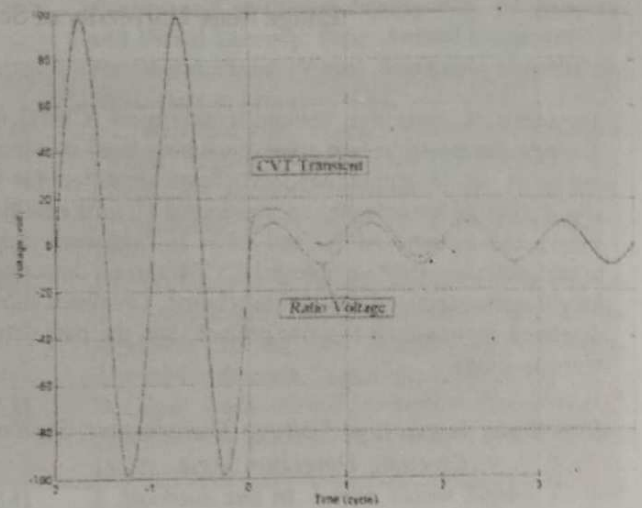


Fig. 4: transient response of a high capacitance CVT

Observation shows that any distance overreach caused by transient output of a higher capacitance CVT is much smaller than that caused by the transient output of a lower capacitance CVT [5].

Fig. 5 shows the effect of higher capacitive CVT on the fundamental voltage magnitude. Result shows a less reduction of fundamental voltage during fault conditions.

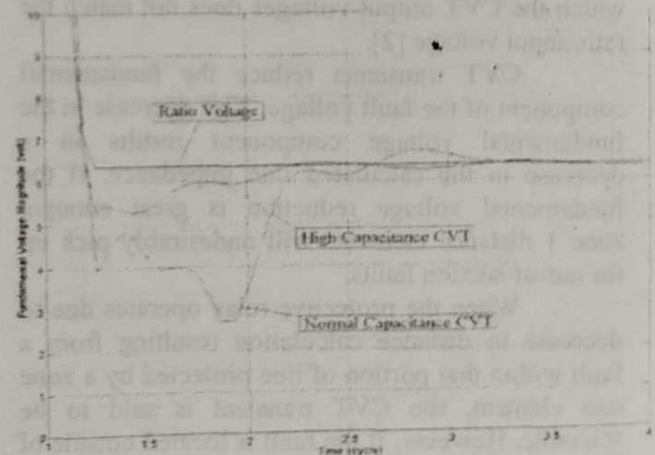


Fig. 5: effect of high capacitance CVT on fundamental voltage magnitude

A ferroresonance suppression circuits, Active ferroresonance suppression circuits (AFSC), and Passive ferroresonance suppression circuits are further added at the secondary output of the CVT to reduce the CVT transients. Fig. 6 shows the AFSC and PFSC configurations while fig. 7 shows how CVT transients are affected by AFSC add PFSC. The resulting indicates that PSFC has a reduced transient than AFSC.

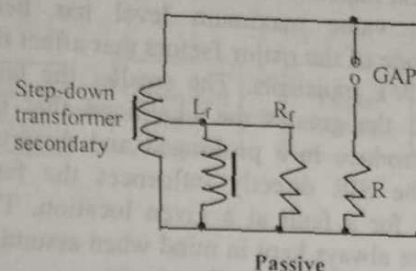
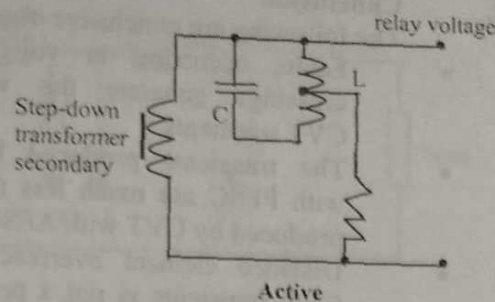


Fig. 6: Active and Passive Ferroresonance-Suppression Circuits

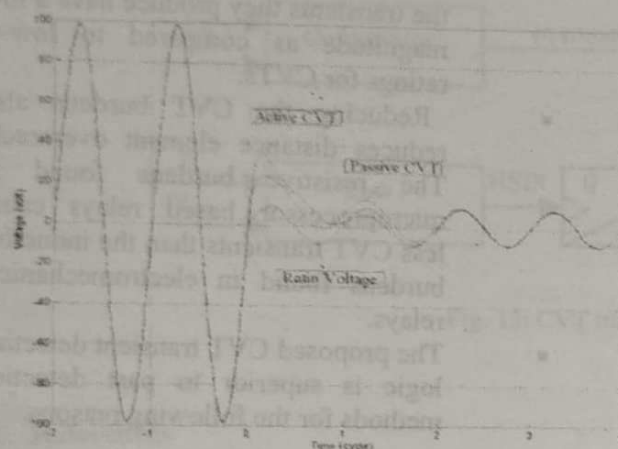


Fig. 7: CVT transients of AFSC and PFSC

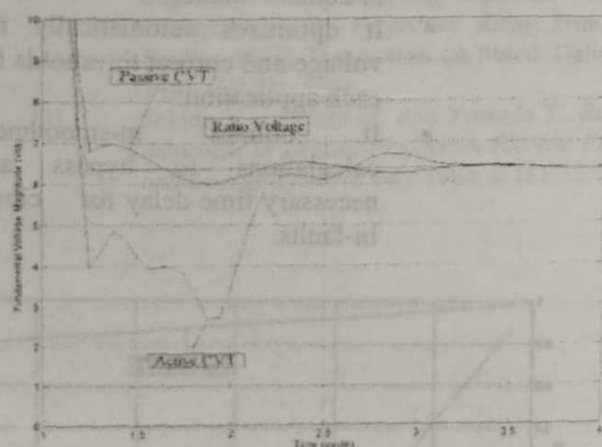


Fig. 8: CVT with PFSC causing less fundamental component reduction.

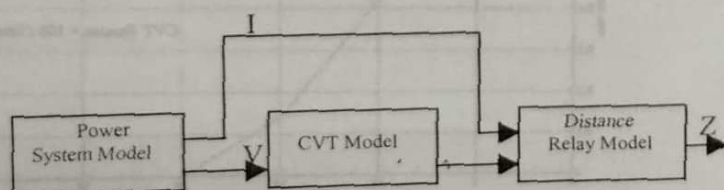


Fig. 9: Distance relay evaluation system

3. Distance Relaying Performance Evaluation during CVT Transients

Fig. 9 below shows a distance relaying evaluation system for determining the performance of distance relay during CVT transients.

3.1 Power System Model

A simple power system model is shown in figure 10. It is a single phase, radial system with a fixed line impedance and variable source impedance. The difference between pre-fault and fault voltage levels heavily affect the CVT transient magnitude and direction. The voltage difference is determined by SIR values, fault locations, and fault resistance (R_f).

3.2 CVT Model

This model assumes the simple CVT structure of fig. 1 with the AFSC and PFSC.

3.3 Relay Model

The relay model used to evaluate the CVT transient includes anti-aliasing low pass filtering, analog-to-digital conversion (decimation), digital band-pass filtering, and impedance calculation (see fig. 11).

3.4 Distance Relay Performance

The generic distance relay performance to transient of CVTs with PFSC and AFSC are shown in fig. 12 below. The fault applied is at the end of the radial line of fig. 10. The curves in the plot show the maximum zone 1 reach setting so as not to pick up due to CVT transients errors.

From these curves, it is observed that the distance relay response for a CVT with a PFSC is much better because the relay has much less overreach. When using a CVT with a PFSC, the need to reduce the zone 1 distance element reach is greatly reduced as compared to that required when using a CVT with an AFSC.

3.5 System Impedance Ratio

Fault value maximum level has been identified as one of the major factors that affect the severity of CVT transients. The smaller the fault voltage level, the greater the likelihood that the CVT will introduce in a prolonged and distorted transients. The SIR directly influences the fault voltage level for a fault at a given location. The SIR values are always kept in mind when assuming the influence of on distance relay.

Fig. 12 equally shows a plot of maximum zone 1 reach setting versus SIR values. When using a CVT having an AFSC, it is observed from the plot that without additional logic, the relay protection must be eliminated for systems with $SIR \geq 20$. The relay transient response employing a CVT with a PFSC is better, with effective zone 1 protection for SIR as high as zero.

4. Improved CVT Transient Detection Logic

So far, it has been shown that generic distance relay has overreach problems [6] when

- The system has a high SIR
- The CVT has an AFSC
- The CVT has low capacitance and heavy inductive burden.

The improved CVT transient detection logic introduces logic that

- Eliminates the distance overreach due to CVT transients.
- Causes maximum time delay for true in-zone faults.
- Requires no special user settings.
- Adapts to different SIRs.

To achieve the above the logic does not follow

- The voltage and current thresholds are automatically calculated by the relay: no factory and user-entered setting are required.
- The distance calculation smoothness is used to defeat the trip time delay for close-in faults on high SIR systems.

Fig. 13 shows the block diagram of the improved CVT transient detection logic.

In the detection logic circuit,

m = distance element calculations

δm = incremental quantity of m

I_0 = elements of phase-to-phase and phase-neutral overcurrents

V_u = elements of phase-to-phase and phase-neutral undervoltage.

T_{DDO} = short time delay.

5. Conclusion

The following are conclusive observations

- Faults occurring at voltage zero-crossings generate the worst-case CVT transients.
- The transients produced by CVTs with PFSC are much less than those produced by CVT with AFSC.
- Distance element overreach due to CVT transients is not a problem for low SIR applications. The statement is equally applicable to CVTs with either AFSC or PFSC.
- High-capacitive CVTs reduce distance element overreach because the transients they produce have a low magnitude as compared to low-C ratings for CVTs.
- Reducing the CVT burdens also reduces distance element overreach. The resistive burdens found in microprocessor based relays cause less CVT transients than the inductive burdens found in electromechanical relays.
- The proposed CVT transient detection logic is superior to past detection methods for the following reasons.
 - It does not require special user or factory settings.
 - It introduces minimum delay for in-zone faults.
 - It optimizes automatically the voltage and current thresholds for each application.
 - It utilizes m-smoothness calculations to bypass any necessary time delay for close-in-faults.

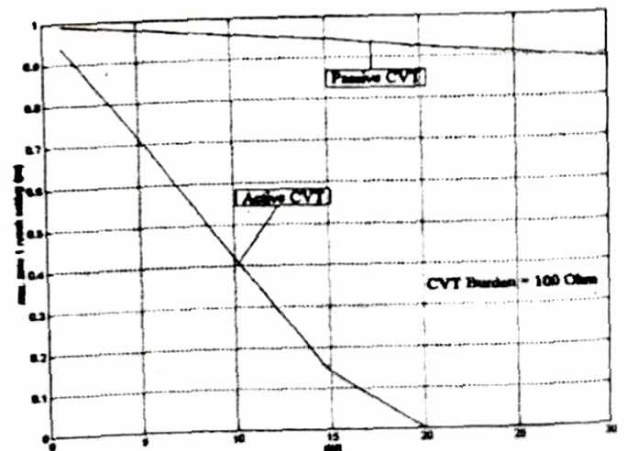


Fig. 12: distance relay performance with AFSC and PFSC.

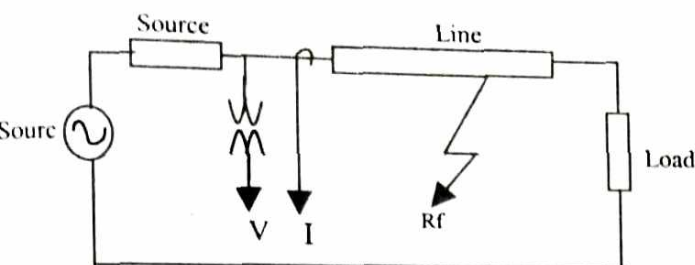


Fig. 10: power system

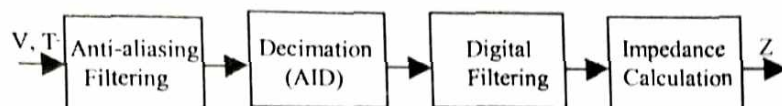


Fig. 11: the relay model

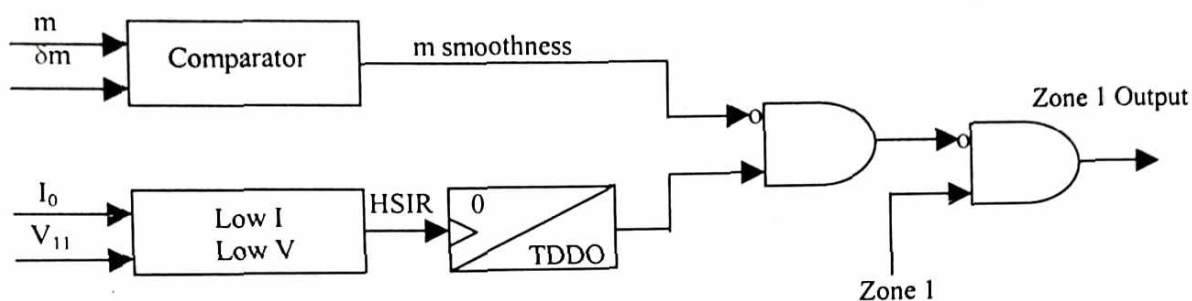


Fig. 13: CVT transient detection logic

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