JEAS

JOURNAL OF ENGINEERING AND APPLIED SCIENCES

Journal of Engineering and Applied Sciences, Volume 19, Number 1, December 2021, 544 - 556

A single-phase voltage boost multilevel inverter topology based on switched - capacitor dc-dc converter: simulation and experimentation

G. C. Diyoke[1*], C. Ezugwu[2] and I. K.Onwuka[3]

[1]Department of Electrical and Electronic Engineering, Michael Okpara University of Agriculture, Umudike, Abia State.

[2]Department of Electrical and Electronic Engineering Technology, Federal Polytechnic, Nasarawa, Nasarawa State.

[3]Department of Electrical and Electronic Engineering, Michael Okpara University of Agriculture, Umudike, Abia State.

[*]CorrespondingAuthor's E-mail: geraldiyoke@mouau.edu.ng

Abstract

The high demand of dc – ac boost power conversion has resulted in the multiplications of many multilevel inverter topologies. This paper presents a simulation and experimental report on single-phase voltage boost multilevel inverter topology based on switched-capacitor dc – dc converter. To keep the power circuit components to a minimum and boost the output voltage, a boost dc – dc converter is connected to a boost switched – capacitor dc – dc converter and finally linked with a conventional full-bridge dc – ac inverter. A low frequency modulation scheme is adopted for both switched-capacitor and full bridge converters. While high frequency switching technique is adopted for the boost converter. Operational principles, mathematical analysis, with MATLAB/Simulink simulation and experimental waveforms are displayed. Assessment of the proposed topology is done by comparing the simulation results with the experimental results. Multilevel inverter output voltage is obtained with a total harmonic distortion of 9.40% at a low single dc input voltage.

Keywords: DC-DC Converter, Multilevel Inverter, Single-phase, Switched-Capacitor, Voltage Boost.

1. Introduction

Due to depletion of the global fossil-energy sources, the development of renewable energy is the most effective solution. However, the available renewable energies such as wind, solar, and fuel cells are reliant on the weather conditions, and their output voltages are low and variable as presented by (Nguyen, Duong and Lim, 2018; Tran *et al.*, 2018). In other to solve the aforementioned drawback of utilizing renewable energies many multilevel inverter topologies have been proposed. As a result of this, many existing multi-level inverters based switched-capacitor circuit (SCC) with H-bridge topologies require large number of power switches and capacitors to construct high numbers of voltage levels (DC multi-level bus voltage) in order to minimize harmonics distortion in AC output voltage have been reported by (Rozlan *et al.*, 2015; Barzegarkhoo *et al.*, 2016; Gupta *et al.*, 2016; Taghvaie, Adabi and Rezanejad, 2016; Zamiri *et al.*, 2016). This can increase the complexity of the control circuit where each power switch is associated with a gate drive unit (opto-isolator), MOSFET drive, and cooling unit (heat-sink). Hence, the overall system will be bulky and costly. Thus, the proposed inverter circuit with a reduced component (power semiconductor switches, diodes, and capacitors) count is introduced. The principle of operation, design and analysis, and control technique of the proposed inverter system are elaborated on in detail. The main idea is to utilize a single low DC input voltage to generate a high ac output voltage with low harmonic content.

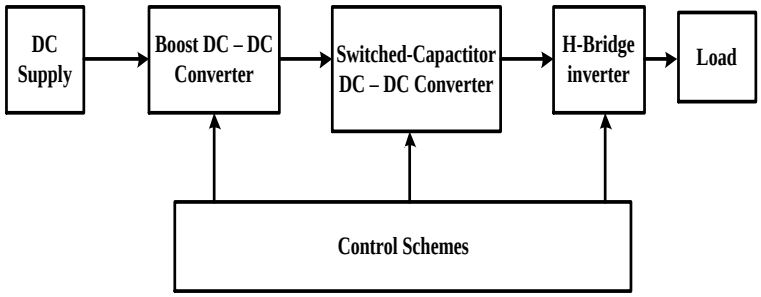

Fig. 1: Block diagram for single-phase voltage boost multilevel inverter topology using boost and switched-capacitor DC - DC converters.

Thus, the proposed inverter system comprises a single dc source voltage, boost dc to dc converter, switched-capacitor dc to dc converter, H-bridge inverter and an open-loop control circuit. Figure 1 shows the block diagram of the proposed inverter system. When the high boost voltage gain is being generated, the boost converter demands to have a large duty cycle, which results to high conduction loss and reducing efficiency (Bratcu *et al.*, 2011; Li and He, 2011; F.S., J.A. and Spiazzi G., 2013). Furthermore, in order to obtain the high boost voltage gain, the various DC-DC converters have been presented, including isolated and non-isolated topologies. The isolated topology as reported in (Ouyang and Sen, 2013; Shi, Jiang and Guo, 2013; Nguyen *et al.*, 2016, 2018) can provide the isolation between input and output terminals, which is based on a high-frequency transformer. Since the isolated topologies include a DC- AC stage and an AC-DC stage, they required a number of components, which increase the circuit's size, weight, cost and reduces its efficiency. The non-isolated topologies (Axelrod, Berkovich and Ioinovici, 2008; Prudente *et al.*, 2008; Yang, Liang and Chen, 2009; Hsieh *et al.*, 2014; Tang, Wang and Fu, 2015; Tang *et al.*, 2016; Hernandez *et al.*, 2017; Nguyen, Duong and Lim, 2018; Padmanaban *et al.*, 2018) can achieve a high efficiency with a simple circuit because of the lack of a transformer. In most of the papers, their duty ratios are always stressed due to the wide range of operation. Also, they contain high harmonic contents which limit their applications. In then on-isolated topologies, the high step-up voltage gain can be achieved by using the following techniques: cascade boost, switched-capacitor, switched-inductor, coupled inductor and a mixture of them. Thus, the aforementioned topologies are limited to DC-DC converters, leakage inductor problems; high number of power switches thereby increasing the gate drive, etc. One merit of some of the configurations is charging of the capacitors in parallel and discharging them in series the switched-capacitor-based converter generates a high voltage at the output side. Furthermore, based on proposed configuration, a conventional boost, switched-capacitor and H-bridge converters are arranged in parallel as shown in Fig. 2. In this arrangement the device count and control complexity decreases.

This paper proposes single-phase voltage boost multilevel inverter topology using boost and switched- capacitor DC - DC converters. This proposed converter topology is derived by combination of two different DC-DC converters and H-bridge inverter. The resulting simplified multilevel inverter require less switches count to provide simultaneous desired multi-level AC with increased output voltage gain. The main features of the proposed converter are as follows: boost dc –dc converter with low duty cycle operating range, a switched –capacitor boost dc – dc converter with limited number of power electronic components, lastly, H-bridge inverter which contains only four power switches. The paper is organized as follows: introduction and block diagram of the proposed topology. Section 2 proposes the materials and method adopted to realize the aim. Such as the operational principle and modulation strategy, and also the Fourier series analysis of the expected output voltage waveform is presented. The computation of switched capacitor DC - DC converter is determined in this section. Thus, the simulation and experimental results are depicted in Section 3, Section 4 shows the research conclusion and finally, some recommendations were made in section 5.

2.0 Material and methods

The materials used were: different converter topology, Oscilloscope, Multimeters, dc voltage source, Matlab/Simulink software, and electrical elements. The methods were: circuit analysis based on three modules, operations, modulation schemes, Fourier analysis of the expected output voltage waveform, computation of capacitor ripple voltages which aids in selection of capacitor values. Fig. 2 shows the proposed multilevel inverter topology with the high-voltage gain. It consists of one DC source, one conventional boost DC - DC converter (inductor(L_m), freewheeling diode (D_m), unidirectional switch (S_m), and two capacitors (C_i and C_o)) one switched-capacitor DC – DC converter (two diodes (D_1 and D_2), two bidirectional switches (S_1 and S_2), H-bridge inverter with

four bidirectional power switches (T_1, T_2, T_3 and T_4), and a resistive-inductive load (*R-L*). To simplify the circuit analyses of the proposed multilevel inverter, Fig. 2 is spilt in three parts as depicted in Fig.3. Thus, the operational waveforms are shown in Fig. 4 and followed by the modulation technique adopted.

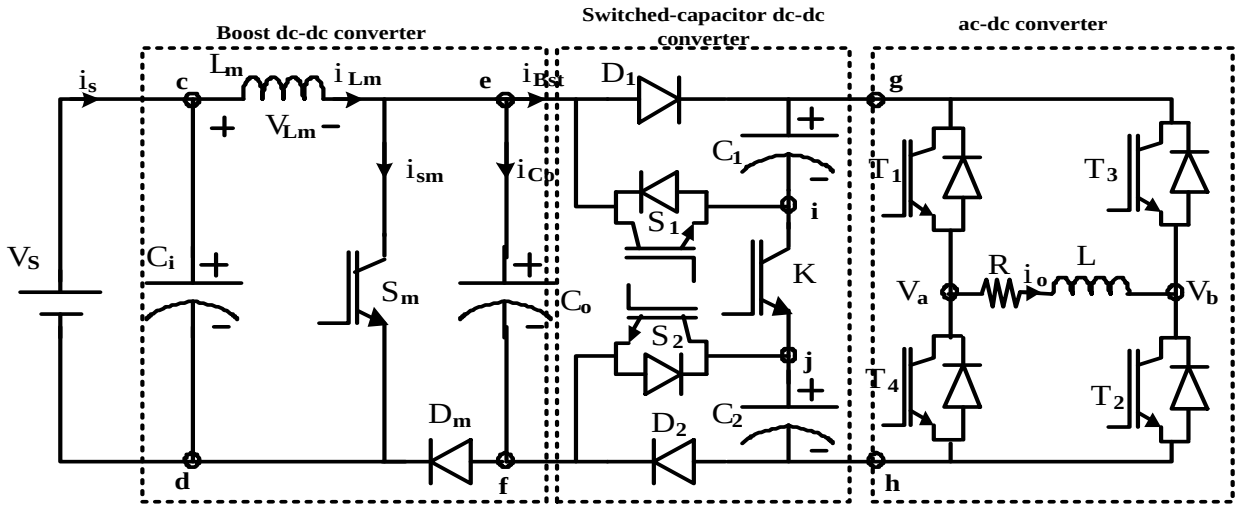

Fig. 2: Complete circuit diagram for the proposed system

2.1 Circuit Configurations

In this subsection, the circuit configurations of the three parts that make up the proposed (single-phase voltage boost multilevel inverter) SPVBMLI topology is displayed in Fig. 3 below.

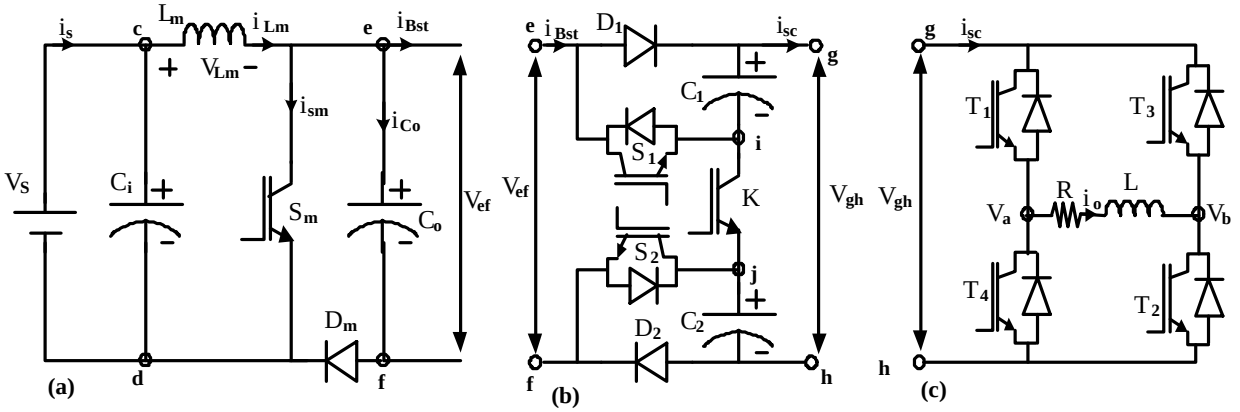

Fig. 3: Circuit configurations: (a) boost dc – dc converter, (b) dc – dc switched-capacitor converter and (c) H-bridge conventional inverter.

Fig. 3(a) depicts the step-up or boost dc to dc converter that has a dc voltage gain V_{ef}/V_s greater than or equal to the dc input voltage. It consists of one inductor (L_m), a freewheeling diode (D_m), a unidirectional power switch and two filtering capacitors. In Fig. 3(b), shows the proposed DC – DC switched-capacitor unit used in this work. As presented in the Figure, the unit consists of two capacitors and two power diodes. Also, two different types of power switches are used in this unit, where S_1 and S_2 switches are bothunidirectional power switches with anti-parallel body diodes and K is a unidirectional power switch for current flow. It has a voltage gain V_{gh}/V_{ef} greater than or equal to DC variable boost output voltage. Fig. 3(c) depicts the H-bridge conventional inverter which consists of four bidirectional power switches (T_1 – T_4) and resistive-inductive load. Here, the output voltage is equal to $(\pm V_{gh})$ input voltage.

2.2 Operational principles

In this subsection, the operational principles of the three parts of that make up the proposed MLI topology is displayed in Fig. 4 below. Boost dc – dc converter inductor voltage and current profile are displayed in Fig. 4(a). The relationship between the input and boost dc voltage i.e. V_{ef} is given as

$$V_{ef} = \frac{V_S}{1 - D} \tag{1}$$

and the current i_{Bst} is given by

$$i_{Bst} = I_S(1 - D) \tag{2}$$

where V_S is the dc input voltage (V), $I_S$is the dc input current, D is the duty cycle, i_{Bst} is dc boost output voltage f_{Sb} dc boost switching frequency.The inductor incremental currentΔi_{Lm} is denoted as

$$\Delta i_{Lm} = \frac{V_S D}{f_{sb} L_m} = \frac{V_{ef} D(1 - D)}{f_{sb} L_m} \tag{3}$$

where L_m is main inductance, V_{ef} is boost converter output voltage.
The maximum value of Δi_{Lm} occurs at D = ½ and is given by

$$\Delta i_{Lm\ max} = \frac{V_{ef}}{4 f_{sb} L_m} \tag{4}$$

The minimum filter inductance L_{mmin} that makes the current conduction just continuous is given by

$$L_{m\ mim} = \frac{R_b(1 - D)^2 D}{2 f_{sb}} \tag{5}$$

The dc boost output voltage ripple can be determined by the change of the charge across the capacitor C_o which is given by

$$\Delta Q = \frac{\Delta I_{Bst}}{f_{sb}} = \frac{\Delta V_S}{f_s(1 - D)R_b} \tag{6}$$

The dc boost ripple voltage ΔV_{co} across the capacitor C_o is

$$\Delta V_{Co} = \frac{\Delta Q}{C_o} = \frac{D V_S}{f_{sb}(1 - D)R_b C_o} \tag{7}$$

Where, C_o is boost output capacitance, R_b is boost resistance.

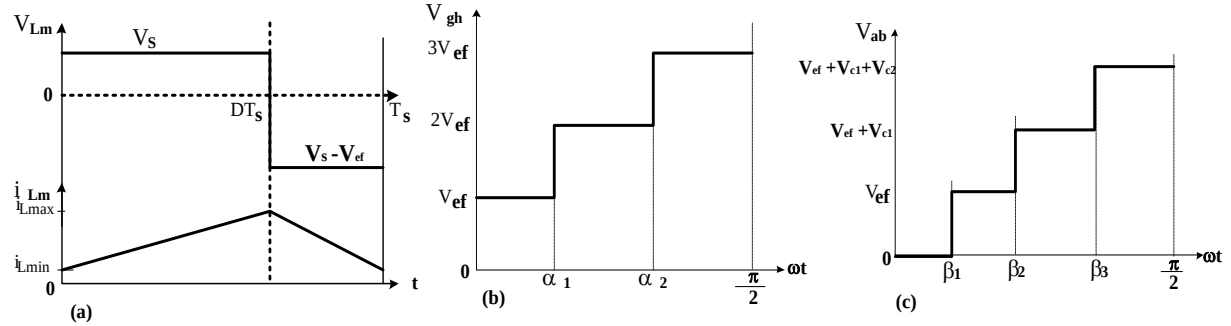

Fig. 4: Ideal waveforms: (a) boost dc – dc converter (b) dc – dc switched-capacitor converter and (c) H-bridge inverter.

Fig.4 (b) depicts the operational interval of a switched capacitor converter.
Mode 1: At the time interval of $0 \leq \omega t \leq \alpha_1$, the power switches S_1, S_2 and K are turned off. The two capacitors C_1 and C_2 are been charged. The voltage drop across V_{gh} becomes V_{ef}. Mathematically,

$$V_{gh} = V_{ef} = \frac{V_S}{1-D} \quad (8)$$

Mode 2a: At the time interval of $\alpha_1 \leq \omega t \leq \alpha_2$, the power switch S_1 is turned off while switches S_2 and K are turned on. The capacitor C_1 charges while C_2 is been discharged. The voltage drop across V_{gh} becomes $2V_{ef}$. Mathematically,

$$V_{gh} = 2V_{ef} = \frac{V_S}{1-D} + \frac{1}{C_2}\int i_{C2}dt \quad (9)$$

Mode 2b: At the time interval of$\pi - \alpha_2 \leq \omega t \leq \pi - \alpha_1$, the power switch S_2 is turned off while switches S_1 and K are turned on. The capacitor C_1 discharges while C_2 is been charged. The voltage drop across V_{gh} becomes $2V_{ef}$. Mathematically, it can be expressed as

$$V_{gh} = 2V_{ef} = \frac{V_S}{1-D} + \frac{1}{C_1}\int i_{C1}dt \quad (10)$$

Mode 3: At the time interval of $\alpha_2 \leq \omega t \leq \frac{\pi}{2}$, the power switches $S_1$and S_2 are turned on while switch K is turned off. The two capacitors C_1 and C_2 are been discharged. The voltage drop across V_{gh} becomes $3V_{ef}$. It can be expressed mathematically as follows

$$V_{gh} = 3V_{ef} = \frac{V_S}{1-D} + \frac{1}{C_1}\int i_{C1}dt + \frac{1}{C_2}\int i_{C2}dt \quad (11)$$

Assuming $i_{c1} = i_{c2} = i_{Bst} = V_S$ (1-D), therefore equation (11) can be simplified as

$$V_{gh} = \frac{V_S}{1-D}\left(1 + \frac{(1-D)^2(C_1+C_2)}{C_1C_2}\int dt\right) \quad (12)$$

Fig.4 (c) depicts the operational interval of H-bridge inverter.
Mode 1: At the time interval of $0 \leq \omega t \leq \beta_1$, the power switches T_1 and T_3 are turned on. The voltage across the load becomes zero. The voltage across the load is expressed as

$$V_{ab} = i_o R + L\frac{di_o}{dt} = 0 \quad (13)$$

Where, R is load resistance, L is load inductance, i_o is output current.
Mode 2a: At the time interval of$\beta_1 \leq \omega t \leq \beta_2$, the power switches T_1 and T_2 are turned on. The voltage across the load becomes equal to V_{ef}. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = V_{ef} \quad (14)$$

Mode 2b: At the time interval of$\beta_2 \leq \omega t \leq \beta_3$, the power switches T_1 and T_2 are turned on. The voltage across the load becomes equal to $2V_{ef}$. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = 2V_{ef} \quad (15)$$

Mode 2c: At the time interval of$\beta_2 \leq \omega t \leq \frac{\pi}{2}$, the power switches T_1 and T_2 are turned on. The voltage across the load becomes equal to $3V_{ef}$. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = 3V_{ef} \quad (16)$$

Mode 3: At the time interval of $\pi \leq \omega t \leq \pi + \beta_1$, the power switches T_2 and T_4 are turned on. The voltage across the load becomes zero. The voltage across the load is expressed as

$$V_{ab} = i_o R + L\frac{di_o}{dt} = 0 \quad (17)$$

Mode 4a: At the time interval of $\pi + \beta_1 \leq \omega t \leq \pi + \beta_2$, the power switches T_3 and T_4 are turned on. The voltage across the load becomes equal to $-V_{ef}$. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = -V_{ef} \quad (18)$$

Mode 4b: At the time interval of $\pi + \beta_2 \leq \omega t \leq \pi + \beta_3$, the power switches T_3 and T_4 are turned on. The voltage across the load becomes equal to $-2V_{ef}$. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = -2V_{ef} \quad (19)$$

Mode 4c: At the time interval of $\pi + \beta_3 \leq \omega t \leq \frac{3\pi}{2}$, the power switches T_3 and T_4 are turned on. The voltage across the load becomes equal to $-3V_{ef}$. Then, the voltage drop across the load becomes

$$V_{ab} = i_o R + L\frac{di_o}{dt} = -3V_{ef} \quad (20)$$

2.3 Modulation scheme

The power circuit configuration in Fig. 2 is an indication that the modulation / control of the power switches should follow suit. Hence, a single pulse modulation scheme is employed in the switching of S_m power switch of dc to dc boost converter. Here, a pulse generator signal with high switching is generated to fire the S_m power switch.
The modulation schemes adopted in switched-capacitor boost dc – dc and dc – ac converters are illustrated in Fig. 5. The reference wave in Fig. 5 is generated from eq. (21). The switching time intervals is computed using eq. (22).

$$V_m = p\sin\omega t \quad \text{and} \quad V_{ref} = |V_m| \quad (21)$$

$$t_1 = \left|\frac{1}{2\pi f}\sin^{-1}\left(\frac{C_{r1}}{p}\right)\right|; \quad t_2 = \left|\frac{1}{2\pi f}\sin^{-1}\left(\frac{C_{r2}}{p}\right)\right|; \; t_3 = \left|\frac{1}{2\pi f}\sin^{-1}\left(\frac{C_{r3}}{p}\right)\right| \quad (22)$$

The modulating sine wave, V_m, is compared with the zero value and the rectified modulating wave, $V_{ref,}$ is compared with three different dc values as depicted in eq. (23). The signals generated are represented as shown in Fig. 5.

$$A = V_m > 0; \quad B = V_{ref} > C_{r3}; \; C = V_{ref} > C_{r2}; \; D = V_{ref} > C_{r1} \quad (23)$$

The switching signals, S_1, S_2, K, and T_1 through T_4, are given by the use of basic logic AND, OR, NOT gates. Their logic expressions are given as follow:

$$S_1 = (A\&B)|\left(\bar{A}\&(B|\bar{D})\right) \quad (24)$$
$$S_2 = (\bar{A}\&C)|\left(A\&(C|\bar{D})\right) \quad (25)$$
$$K = (\bar{B}\&C)|\bar{D} \quad (26)$$

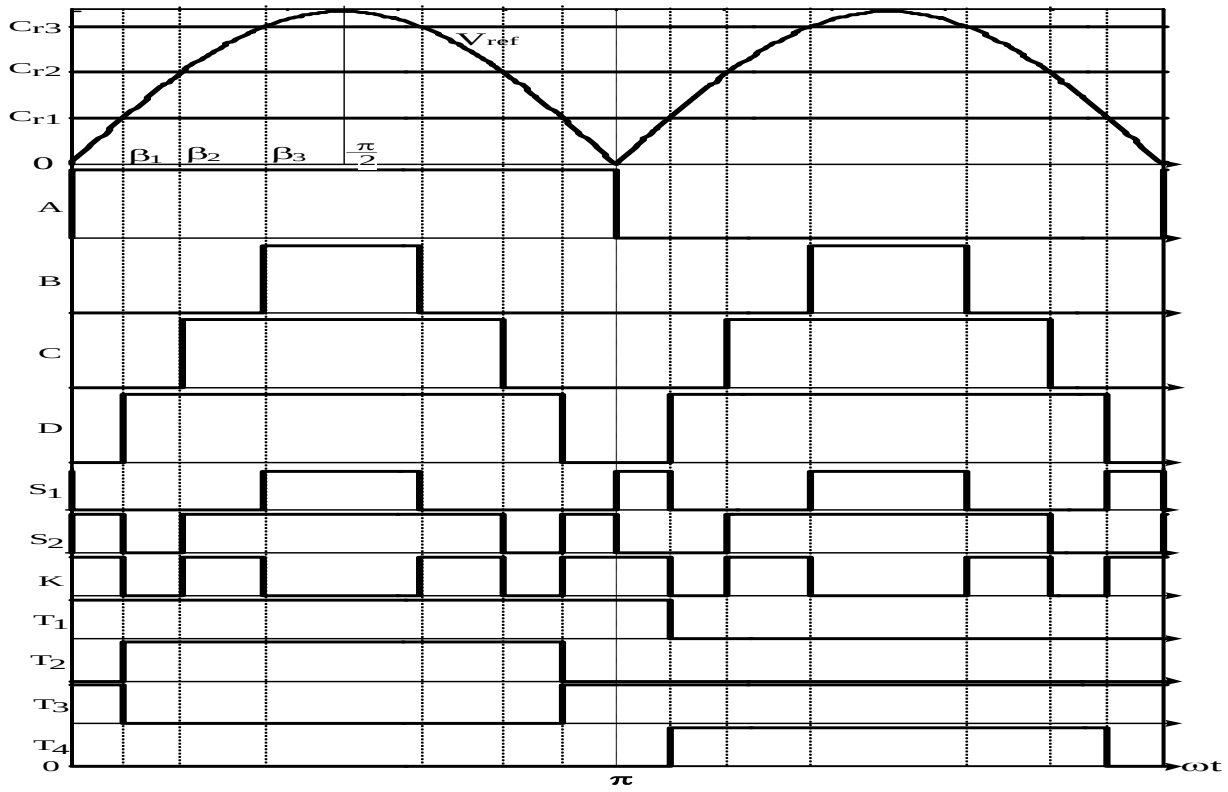

Fig. 5: Operational waveforms of the connected switched-capacitor inverter.

Where, V_{ref} = absolute modulation reference voltage, $V_{m\,=}$ ac modulation reference voltage, C_{r1}, C_{r2} and C_{r3} = carrier voltages levels. β= switching angle, P = peak modulation voltage.

$$T_2 = A\&D; \quad T_4 = \bar{A}\&D; \; T_1 = \bar{T}_4; \; T_3 = \bar{T}_2 \tag{27}$$

2.4 Fouries Analysis

The staircase output V_o or V_{ab} can be divided into four components $0V_S$; $\frac{V_S}{1-D}$; $\frac{2V_S}{1-D}$; and $\frac{3V_S}{1-D}$, as shown in Fig. 6. The durations of each component are decided by the comparisons of each dc signal (C_{r1}, C_{r2} and C_{r3}) and rectified sine wave (V_{ref}). If pulse widths of the constituted component are defined as δ_1, $\delta_1+\delta_2$, and $\delta_1+\delta_2+\delta_3$, Fourier analysis is accomplished for this staircase as shown in eq. (28).

$$V_{ab}(\omega t) = \begin{Bmatrix} V_{ab\,1}(\omega t) = 0V_s; \;\; 0 \le \omega t \le \delta_1 \\ V_{ab\,2}(\omega t) = \frac{V_S}{1-D}; \;\; \delta_1 \le \omega t \le \delta_1 + \delta_2 \\ V_{ab\,3}(\omega t) = \frac{2V_S}{1-D}; \;\; \delta_1 + \delta_2 \le \omega t \le \delta_1 + \delta_2 + \delta_3 \\ V_{ab\,4}(\omega t) = \frac{3V_S}{1-D}; \;\; \delta_1 + \delta_2 + \delta_3 \le \omega t \le \frac{\pi}{2} \end{Bmatrix} \tag{28}$$

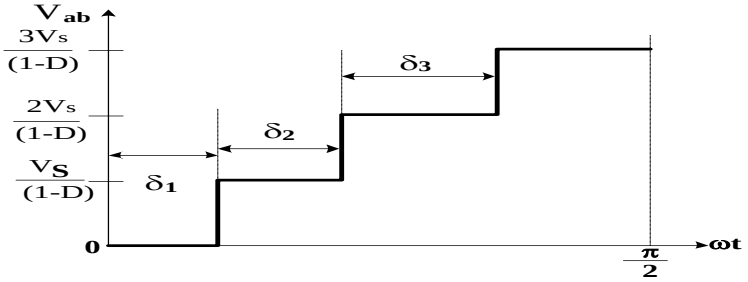

Fig. 6: Output voltage decomposition for Fourier analysis.

In general, we have the expression of Fourier series as

$$V_{ab}(\omega t) = \sum_{n=1}^{\infty} b_n \sin n\omega t \quad (29)$$

For $a_o = a_n$ = zero; thus, considering the waveform as an odd quarter-wave and b_n can be evaluated as

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} V_{abn}(\omega t)\sin n\omega t d\omega t \quad (30)$$

Putting eq. (28) into eq. (30) and solving yields eq. (31)

$$b_n = \frac{4V_S}{n(1-D)\pi}(\cos n\delta_1 + \cos n(\delta_1+\delta_2) + \cos n(\delta_1+\delta_2+\delta_3)) \quad (31)$$

where, δ_1, δ_2 and $\delta_3$are pulse width angles, n = number of harmonic content
The voltage total harmonic distortion (THD_v) can be expressed as

$$THD_v = \frac{(1-D)\pi}{4V_S(\cos\beta_1+\cos\beta_2+\cos\beta_3)}\sqrt{\sum_{n=1,3,5,\ldots}^{\infty}\left(\frac{4V_S}{n(1-D)\pi}[\cos n\beta_1+\cos n\beta_2+\cos n\beta_3]\right)^2} \quad (32)$$

where, $\beta_1 = \delta_1$; $\beta_2 = \delta_1+\delta_2$; $\beta_3 = \delta_1+\delta_2+\delta_3$.

$$V_{ab}(\omega t) = \sum_{n=1,3,5,\ldots}^{\infty}\frac{4V_S}{n(1-D)\pi}(\cos n\beta_1+\cos n\beta_2+\cos n\beta_3)\sin n\omega t \quad (32a)$$

If the load is resistive-inductive element, the load current can be expressed by

$$i_{ab}(\omega t) = \frac{4V_S}{(1-D)\pi}\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{nZ_n}(\cos n\beta_1+\cos n\beta_2+\cos n\beta_3)\sin n(\omega t-\varphi_n) \quad (33)$$

The change in the capacitor voltages is given by

$$\Delta V_{Ceq} = \frac{1}{C_{eq}}\int_{t_3}^{\frac{1}{2f}-t_3} i_{ab}(t)dt \quad (34)$$

Putting eq. (33) into eq. (34) and simplifying the expression, the ripple voltage is determined as

$$\Delta V_{Ceq} = \frac{4V_S(C_1+C_2)}{\pi^2 fZ(1-D)C_1C_2}(\cos\beta_1+\cos\beta_2+\cos\beta_3)(\cos\varphi_1\cos(2\pi ft_3)) \quad (35)$$

The capacitor stored charge can be evaluated as follows

$$Q_{Ceq} = \frac{4V_S}{\pi^2 fZ(1-D)}(\cos\beta_1+\cos\beta_2+\cos\beta_3)(\cos\varphi_1\cos(2\pi ft_3)) \quad (36)$$

It can be ascertained that some factors affect the capacitor ripple voltage value such as input voltage, load frequency, load impedance, load angle, duty cycle, and switching angles or times. So, it is very vital to be mindful in selection of the aforementioned parameters

3.0 Results and Discussions

Computer aided simulation based on MATLAB/SIMULINK is performed for the proposed topology. The simulation specification parameters are depicted in a Table 1. Also, the simulation results are validated using experimental results as presented in this section.

3.1 Simulation Results

Fig. 7 (a) through (h) show the simulated voltage drop waveforms across some circuit elements in dc- dc boost converter under a steady state. Fig. 7(a) depicts the step dc input voltage, the boost dc-dc output voltage is shown in Fig. 7(b), voltage across boost inductor is as indicated in Fig. 7(c), Fig. 7(d) shows the voltage drop across the

capacitor of the boost converter. Voltage drop and current flow through the freewheeling diode in the boost converter are depicted in Figs. 7(e) and 7(g) respectively. Also, the inductor and boost output currents are shown in Figs. 7(f) and 7(h) respectively.

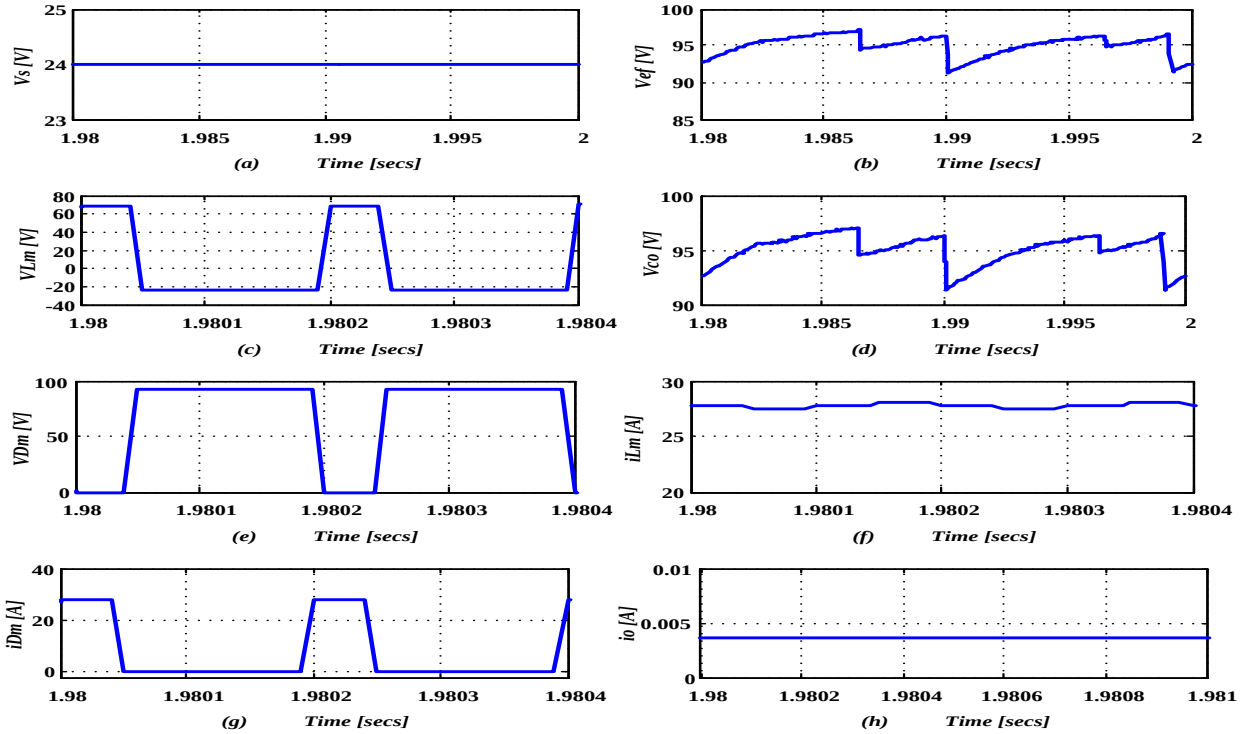

Fig. 7: Waveforms: (a) dc input voltage, (b) dc – dc output voltage, (c) voltage drop across the inductor, (d) voltage drop across the capacitor, (e) voltage drop across the diode (f) inductor current, (g) diode current and (h) boost dc – dc output current.

Fig. 8 (a) through (g) show the simulated voltage drop waveforms across some power switches in dc- dc boost converter under a steady state. Fig. 8(a) depicts the blocking voltage across the switch S_1, the blocking voltage across S_2 is shown in Fig. 8(b), the voltage across the switch K is as indicated in Fig. 8(c), Fig. 8(d) shows the blocking voltage drop across the switch T_1. Fig. 8(e) shows the blocking voltage drop across the switch T_2. Switches T3 and T4 blocking voltages are displayed respectively in Figs. 8(f) and 8(g). Fig. 9 shows the simulated output voltage and current waveforms across load in switched-capacitor dc- dc converter under a steady state. The simulated output voltage resultis in line with the theoretical analysis. Also, the output current under resistive-inductive load was shifted by the load angle as depicted in Fig. 9. Fig. 10 shows the fast Fourier transform (FFT) of the output voltage which contains smaller fractions of lower order harmonics.

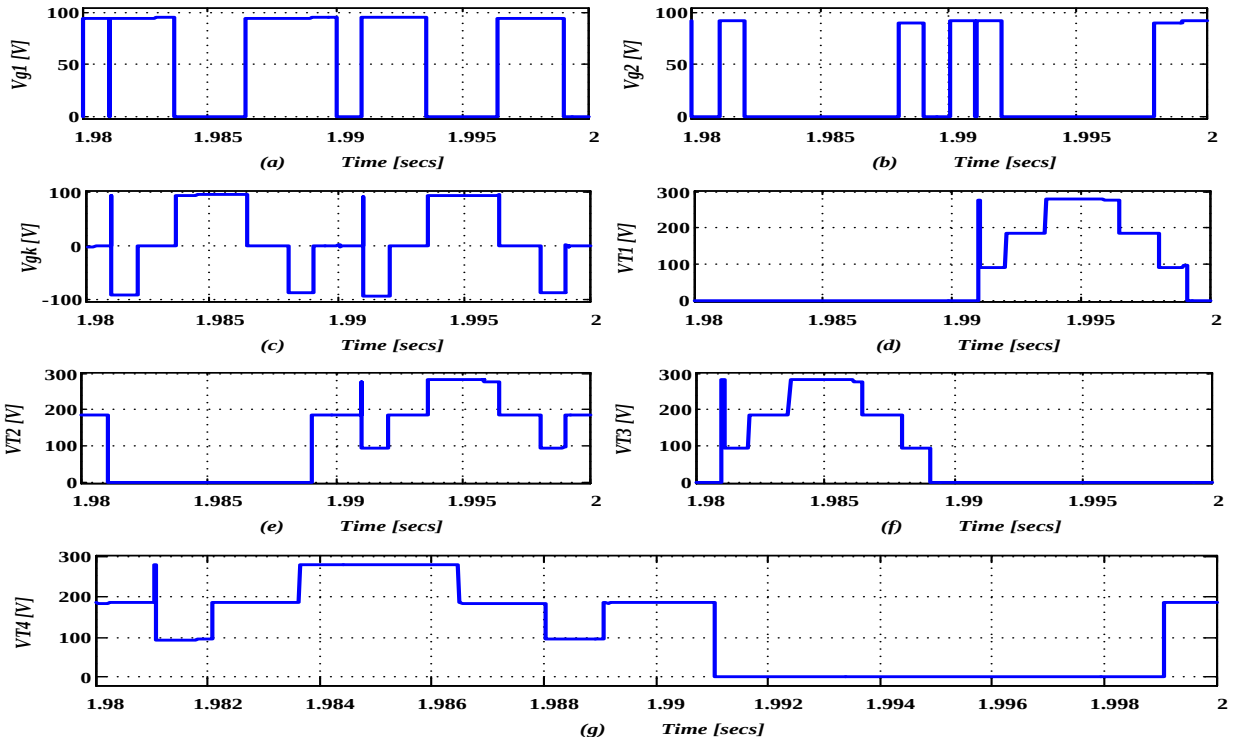

Fig. 8: Switch voltage waveforms for low frequency modulation scheme: (a) S_1, (b) S_2, (c) K, (d) T_1, (e) T_2, (f) T_3, and (g) T_4.

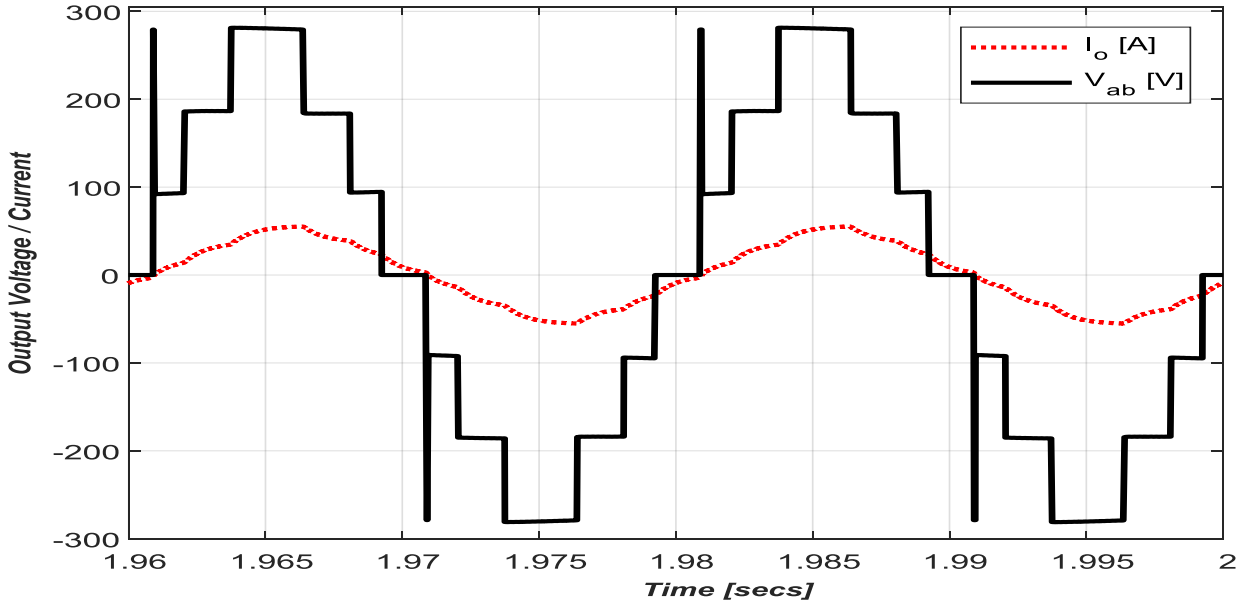

Fig. 9: Waveforms of inverter output voltage, and inverter output current.

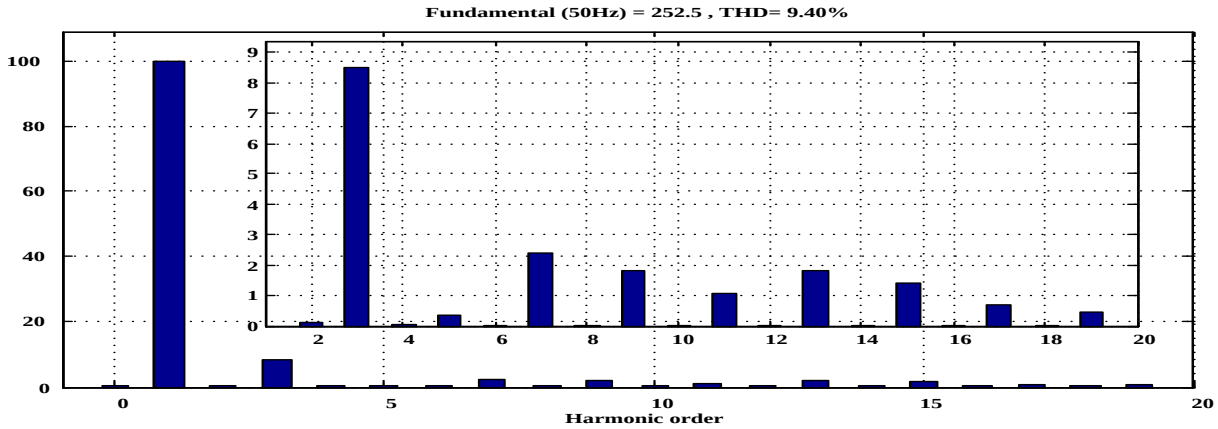

Fig. 10: Harmonic profile of the output voltage of the proposed system.

3.2 Experimental Results

In line with the simulation results, a laboratory prototype was built in the Power Electronics Laboratory and the prototype specifications and parameters are given in Table 2.

Table 1. Simulation circuit parameters

Paramters	Values
V_s	24V
D	0.75
C_{r1}, C_{r2} and C_{r3}	0.3V, 0.6V and 0.9V
P	1V
f, f_s&f_{sb}	50 Hz, 2kHz & 5kHz
$C_1 = C_2$	3900uF by 100V
L_m	5mH
R_o	50 ohms
L_o	40mH

Table 2. Experimental circuit parameters

Parameters	Values
V_s	12V
D	0.75
C_{r1}, C_{r2} and C_{r3}	0.3V, 0.6V and 0.9V
P	1V
f	50Hz
f_{sb}	23kHz
$C_1 = C_2$	3900uF by 100V
L_m	5mH
R_o	68 ohms
Power switches	IRF460N

Fig. 11 depicts the system output voltage waveform under a resistive load. Indeed, this shows a seven level inverteroutput voltage waveform operating at a fundamental frequency of 50 Hz with voltage magnitude of 105 Vac.

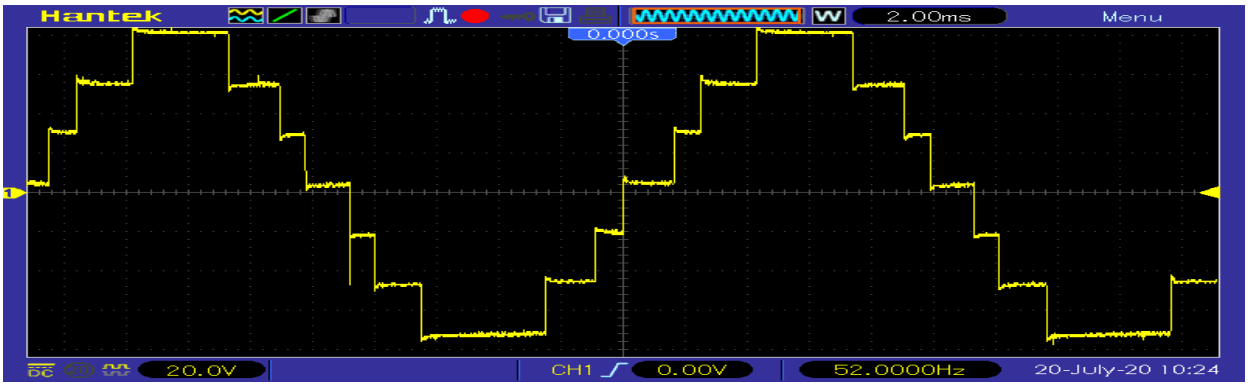

Fig. 11: Experimental ac output voltage, V_{ab} of the proposed system.

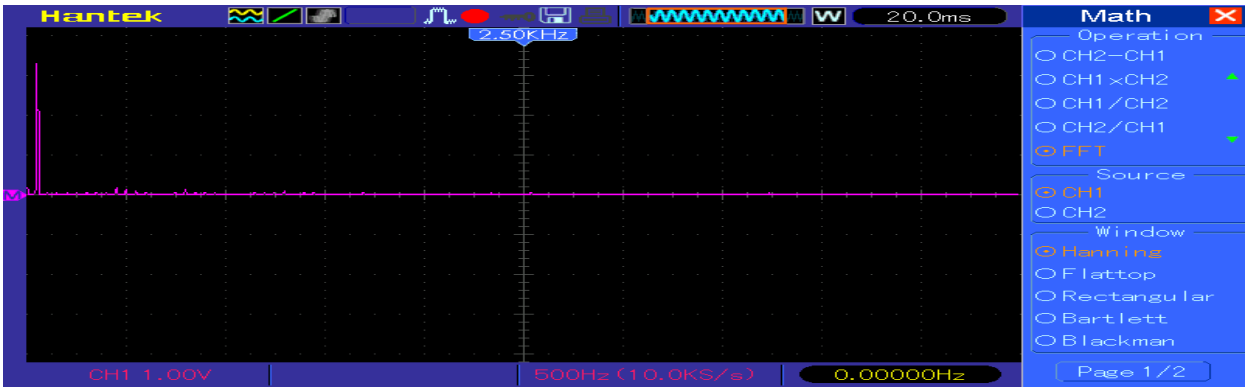

Fig. 12: Harmonic profile of the output voltage of the proposed system.

Fig. 12 shows the experimental harmonic profile of the proposed output voltage. The fast Fourier transform analysis was performed on the output voltage waveform both in simulation and experimental forms. The result in Fig. 10 depicts simulation total harmonic distortion (THD) content of 9.40% and Fig. 12 shows the experimental THD content of 9.62%, therefore, these values fall within the IEEE standard value.

4.0. Conclusion

This paper presented both computer aided simulation and experimental reports on a single-phase voltage boost multilevel inverter topology based on switched – capacitor dc – dc converter. It was observed that a reduced harmonic content and a boosted output voltage were obtained. The mathematical analysis, operational principles, computer simulation and experimental switching functions were depicted. Analyses of the output voltage waveforms from the laboratory prototype as in Fig. 11 of the proposed topology validate mathematical model depicted in Fig. 4(c) and simulation results as shown in Fig. 9. The little discrepancy that existed between the simulation and experimental results are due to little variation in circuit parameters.

5.0 Recommendation

Several possible extensions of this work are presented as (i) generation of gating signals adopting sinusoidal pulse width modulation scheme, (ii) implementation of the switching technique using digital programmable chip such as PIC 16F627A, (iii) three-phase implementation of the work can be carried out.

Acknowledgement

The authors wish to acknowledge staff of the Department of Electrical and Electronic Engineering, Michael Okpara University of Agriculture, Umudike for the contributions made towards the success of the work.

References

Axelrod, B., Berkovich, Y. and Ioinovici, A. 2008. 'Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters', *IEEE Trans. Circuits Syst. I*, 55, pp. 687–696.

Barzegarkhoo, R., Zamiri, E., Vosoughi, N., Kojabadi, H.M. and Chang, L., 2016. Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count. *IET Power Electronics*, *9*(10), pp.2060-2075..

Bratcu, A.I., Munteanu, I., Bacha, S., Picault, D. and Raison, B., 2010. Cascaded dc–dc converter photovoltaic systems: Power optimization issues. *IEEE Transactions on Industrial Electronics*, *58*(2), pp.403-411..

Garcia, F.S., Pomilio, J.A. and Spiazzi, G., 2012. Modeling and control design of the interleaved double dual boost converter. *IEEE Transactions on Industrial Electronics*, *60*(8), pp.3283-3290.

Gupta, K.K., Ranjan, A., Bhatnagar, P., Sahu, L.K. and Jain, S., 2015. Multilevel inverter topologies with reduced device count: A review. *IEEE transactions on Power Electronics*, *31*(1), pp.135-151.

Villarreal-Hernandez, C.A., Mayo-Maldonado, J.C., Valdez-Resendiz, J.E. and Rosas-Caro, J.C., 2017, July. Modeling and control of an interleaved DC-DC multilevel boost converter. In *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)* (pp. 1-6). IEEE.

Hsieh, Y.P., Chen, J.F., Yang, L.S., Wu, C.Y. and Liu, W.S., 2013. High-conversion-ratio bidirectional DC–DC converter with coupled inductor. *IEEE Transactions on Industrial Electronics*, *61*(1), pp.210-222

Li, W. and He, X. 2011. 'Review of non-isolated high-step-up DC/DC converters in photovoltaic grid-connected applications', *IEEE Trans. Ind. Electron*, 58, pp. 1239–1250.

Nguyen, M.-K., Duong, T.-D. and Lim, Y.-C. 2018 'Switched-Capacitor-Based Dual-Switch High-Boost DC–DC Converter', *IEEE Transactions on Power Electronics*, 33(5), pp. 4181–4189.

Nguyen, M.K., Lim, Y.C., Choi, J.H. and Cho, G.B., 2016. Isolated high step-up DC–DC converter based on quasi-switched-boost network. *IEEE Transactions on Industrial Electronics*, *63*(12), pp.7553-7562.

Nguyen, M.K., Duong, T.D., Lim, Y.C. and Kim, Y.J., 2018. Isolated boost DC–DC converter with three switches. *IEEE Transactions on Power Electronics*, *33*(2), pp.1389-1398..

Ouyang, Z. and Sen, G. 2013 'Thomsen, O.C.; Andersen, M.A.E. Analysis and design of fully integrated planar magnetics for primary–parallel isolated boost converter', *IEEE Trans. Ind. Electron*, 60, pp. 494–508.

Padmanaban, S., Bhaskar, M.S., Maroti, P.K., Blaabjerg, F. and Fedák, V., 2018. An original transformer and switched-capacitor (T & SC)-based extension for DC-DC boost converter for high-voltage/low-current renewable energy applications: Hardware implementation of a new T & SC boost converter. *Energies*, *11*(4), p.783.

Prudente, M., Pfitscher, L.L., Emmendoerfer, G., Romaneli, E.F. and Gules, R., 2008. Voltage multiplier cells applied to non-isolated DC–DC converters. *IEEE Transactions on Power Electronics*, *23*(2), pp.871-887.

Rozlan, M.H., Darwish, M.K., Sallama, A. and Khodapanah, M., 2015, September. Low loss inverter circuit based on buck and boost topology. In *2015 50th International Universities Power Engineering Conference (UPEC)* (pp. 1-5). IEEE.

Shi, X., Jiang, J. and Guo, X. 2013. 'An efficiency-optimized isolated bidirectional DC-DC converter with extended power range for energy storage systems in microgrids', *Energies*, 6, pp. 27–44.

Taghvaie, Adabi, J. and Rezanejad, M. 2016. 'Circuit Topology and Operation of a Step-Up Multilevel Inverter with a Single DC Source', *IEEE Transactions on Industrial Electronics*, 63(11), pp. 6643–6652.

Tang, Y., Fu, D., Kan, J. and Wang, T., 2015. Dual switches DC/DC converter with three-winding-coupled inductor and charge pump. *IEEE Transactions on Power Electronics*, *31*(1), pp.461-469.

Tang, Y., Wang, T. and Fu, D. 2015. 'Multicell switched-inductor/switched-capacitor combined active-network converters', *IEEE Trans. Power Electron*, 30, pp. 2063–2072.

Tran, V.T., Nguyen, M.K., Choi, Y.O. and Cho, G.B., 2018. Switched-capacitor-based high boost DC-DC converter. *Energies*, *11*(4), p.987.

Yang, L. S., Liang, T. J. and Chen, J. F. 2009. 'Transformerless DC-DC converters with step-up voltage gain', *IEEE Trans. Ind. Electron*, 56, pp. 3144–3152.

Zamiri, E., Vosoughi, N., Hosseini, S.H., Barzegarkhoo, R. and Sabahi, M., 2016. A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components. *IEEE Transactions on Industrial Electronics*, *63*(6), pp.3582-3594.